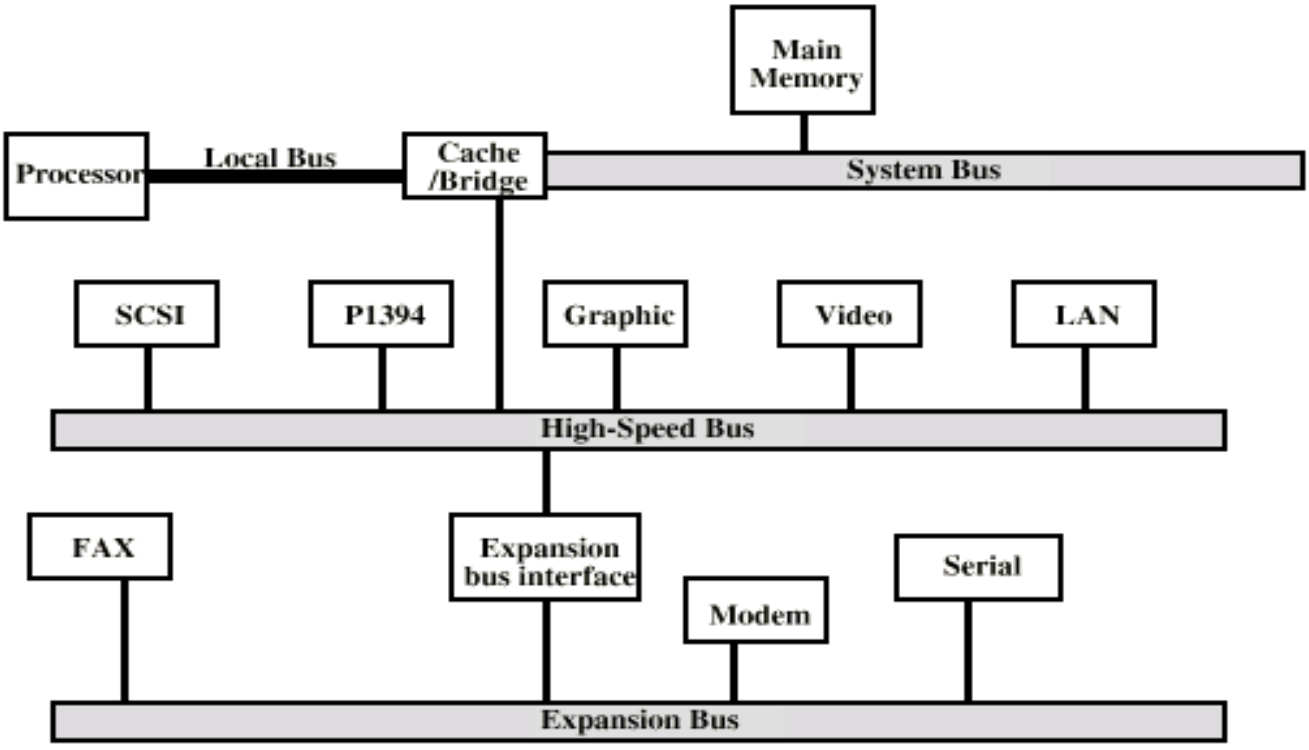
ECP2046 Computer Organization and Architecture
SOLUTION FOR TUTORIAL 3

Q1. The shortcomings of the traditional bus architecture:

As higher and higher performance is seen in the I/O devices, it begins to break down. The high-speed devices are not brought into closer integration with the processor. In general, if more devices are attached to the bus, it will increase the bus length and this will in turn increase propagation delay. This delay will affect the performance.

In response to the growing demands, a common approach, taken by industry is to build high-speed bus that is closely integrated with the rest of the system, requiring only a bridge between the processor's bus and the high-speed bus. This arrangement is shown below which is sometimes known as a mezzanine architecture.



The advantage of this arrangement is that the high-speed bus brings high-demand devices into closer integration with the processor and at the same time is independent of the processor. Thus, differences in processor and high-speed bus speeds and signal line definitions are tolerated. Changes in processor architecture do not affect the high-speed bus and vice versa.

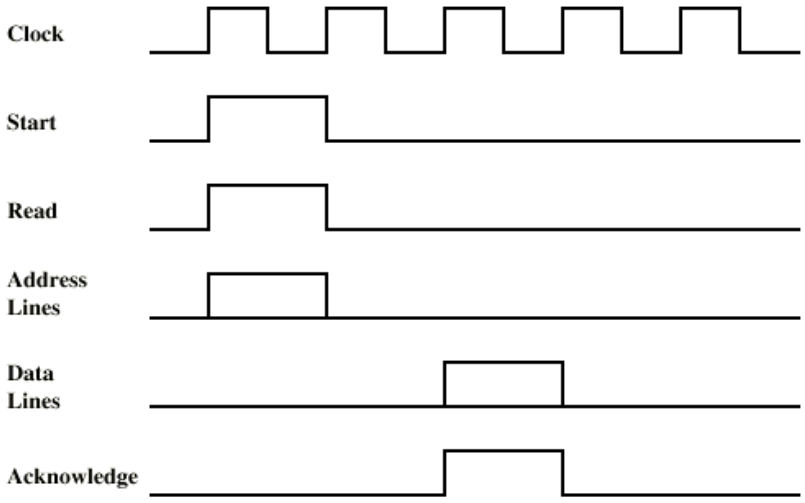
Q2. The factors to be considered in the implementation of a bus are the following:

i. Bus types --- dedicated or multiplexed.
ii. Method of arbitration—centralized or distributed
iii. Timing --- synchronous or asynchronous
iv. Bus width--- 8 or 16 or 32 bits
v. Data transfer type

Q3. The advantage of time multiplexing the data and address buses will be the use of fewer lines. This will save space and reduce the cost.
The disadvantage is that more complex circuitry is needed in each module as additional control is required for demultiplexing. Also, there is a potential reduction in performance because certain events that share the same lines cannot take place in parallel.

Q4. With synchronous bus, the occurrence of events on the bus is determined by a clock. In asynchronous bus, the occurrence of one event on the bus follows and depends on the occurrence of a previous event.
Synchronous timing is simpler to implement and test. However it is less flexible than asynchronous timing. Because all devices on a synchronous bus are tied to a fixed clock rate, the system cannot take advantage of advances in device performance. With asynchronous timing, a mixture of slow and fast devices, using older and newer technology, can share a bus.

Q5.



Timing Diagram for a Synchronous Read operation

The processor issues a read signal and places the memory address on the address bus. It also issues a start signal to mark the presence of address and control signals on the bus. A memory module recognizes the address and after a delay of one cycle, places the data and an acknowledgement signal on the bus.